# AN-707

Application Note



# NOISE IMMUNITY COMPARISON OF CMOS VERSUS POPULAR BIPOLAR LOGIC FAMILIES

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This Application Note compares the noise immunities of the four major logic families used today in industrial logic systems designs: TTL, DTL, HTL, and CMOS. Also included are general discussions of common noise sources, precautions against noise, noise specification, and standard noise tests.

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## INTRODUCTION

Widespread use of digital logic systems in many industrial applications has created an increasing demand for insight into the special noise considerations and precautions required to operate reliably in a noisy industrial environment. The question that invaribly arises when selecting a logic family for an industrial application is "What is the family's noise immunity, and how does it compare with that of the other logic families?"

In answer to that question, many articles and papers have been written comparing the noise immunity of the TTL (transistor-transistor logic), DTL (diode-transistor logic), and HTL (high-threshold logic) families. This article compares the noise immunity of CMOS (complementary metal-oxide-semiconductor), a relatively new logic family that has been enthusiastically received by industrial logic designers with the noise immunities of those other families.

Included is a discussion of the various types of noise, common methods of protecting a logic system from noise, and accepted tests performed to determine how inherently "immune" a family is to noise. Graphs and tables of data comparing the "d-c noise margin," "a-c noise immunity," and "noise-energy immunity" of the TTL, DTL, HTL, and CMOS logic families, as well as the interpretation of those graphs under actual operating conditions are also discussed.

## NOISE SOURCES

Sources of electrical noise may be classified as either external or internal to a digital logic system. External noise may be generated by electric motors, arcing relay contacts, circuit breakers, etc. This noise is usually in the form of randomly generated spikes of electromagnetic interference, that couples inductively to the power, ground, and signal inter-connections within the logic system. Internal noise may be generated on the signal lines by crosstalk (capacitive coupling between adjacent signal lines), on transmission lines from reflections (due to impedance mismatch), and on the power and ground lines by current surges occuring during switching.

Some of the external noise generators mentioned may generate voltages in the neighborhood of thousands of volts. This voltage would, of course, disturb any integrated circuit existing today. Fortunately, this amount of voltage is usually never applied directly to any digital circuit line. Rather, it must couple through the very high impedance of free space. Therefore, the total energy (thus voltage) absorbed by the signal line is dependent on the ratio of the coupling impedance (free space) to the digital circuit impedance of the signal, power and ground lines. If the circuit line impedances are very low compared to the coupling impedance, even high voltage noise sources should have little effect on the circuit; however, to determine the effect of external noise generators requires a knowledge of the generated energy, coupling impedance, circuit line impedances, circuit noise-margin, and circuit speed.

The effect of internally generated noise on circuit operation also depends on the noise margin, speed, and impendance of the circuit. Unless long lines are being driven, the effects of cross talk and transmission-line reflections are minimal in all logic families except the superfast ECL (emitter coupled logic) family. Power and ground noise is due primarily to poor power and ground returns in the system, and internally generated noise on the power and ground lines seems to be a significant effect only in systems using logic with very fast rise and fall times.

## NOISE PRECAUTIONS

There are two approaches for dealing with electrical noise in digital logic modules in a noisy industrial environment: (1) keeping the noise out of the system and (2) minimizing the influence of noise that does get into the system.

Here are some system design and construction practices commonly used to keep noise out:

1. Segregate logic wiring from field* wiring. Do not design input converters and output drivers so that field wiring uses the same connectors that carry logic signals. Arrange to use opposite ends of printed boards for logic and field-wiring connections, and never allow the both types of wiring to be adjacent or to be bundled together.
2. Do not mix logic grounds with field grounds. This does not mean that logic ground should float; however, heavy currents should not pass through the logic system ground on the return path to the power supply. An excellent scheme is to switch the a-c line with optically isolated triacs. D-C solenoid

(*) The term "field" is used here to refer to high power interface circuitry (either semiconductor or electromechanical) which is external to (and possibly controlled by) the logic module.

drivers might seem difficult to isolate, but judicious use of ground-isolating resistors and auxiliary chassis tie points can force most of the load current outside the logic system ground.

3. Use high density packaging. Computer-type modular construction minimizes lead lengths in the logic, reducing the coupling between logic wiring and nearby field wiring. Dense packing also cuts resistance and inductance in the logic ground system, minimizing interference from residual noise currents that may be present. Select a logic family with a strong complement of MSI (medium scale integration) functions, this will improve packing density.
4. Where logic and power circuits must be adjacent, use shielding. For example, a group of printed circuit boards carrying field circuits can be shielded from general-purpose logic modules by inserting unetched copper-clad boards in the sockets that separate the two groups.
5. Filter the line voltage where it enters the logic power supply, and at the supply output terminals. Bypass capacitors, typically 100 pF silver mica to remove high frequency transients and 0.1$\mu$F ceramic to remove lower frequency transients, should be used wherever power supply lines enter the circuit board.

One of the best ways to minimize the effects of noise that may enter a logic system, in spite of the previously mentioned precautions, is to design with a family that has good noise-rejection characteristics. Therefore, the inherent noise immunity of the logic family should be considered in addition to the usual considerations such as cost, speed, availability, and compatibility. Here are some considerations that should be taken into account when selecting a logic family to operate in a hostile industrial noise environment:

1. Slower speed or longer propagation delay logic families are usually less susceptible to noise, since noise is generally more intense at higher-frequencies (MHz range). Metal-to-metal contacts are nearly ideal step generators, and wiring resonances often generate high frequency noise peaks.
2. Logics requiring fast rise and fall time inputs are more inherently sensitive to high-frequency noise than slower rise time logic families that switch by level sensing rather than edge sensing.
3. Using complex MSI and LSI functions in a logic system can reduce the number of circuit components and interconnection lines into which noise can be coupled. Also, complex functions usually reduce the total system cost, since fewer individual components must be assembled.
4. Inherently fast rise and fall time logic generates large current spikes internally on system power and ground lines. Slower logic greatly reduces this problem.
5. High noise-voltage margins and low signal line impendances are good insurance against noise. These features are discussed and characterized in the following sections.

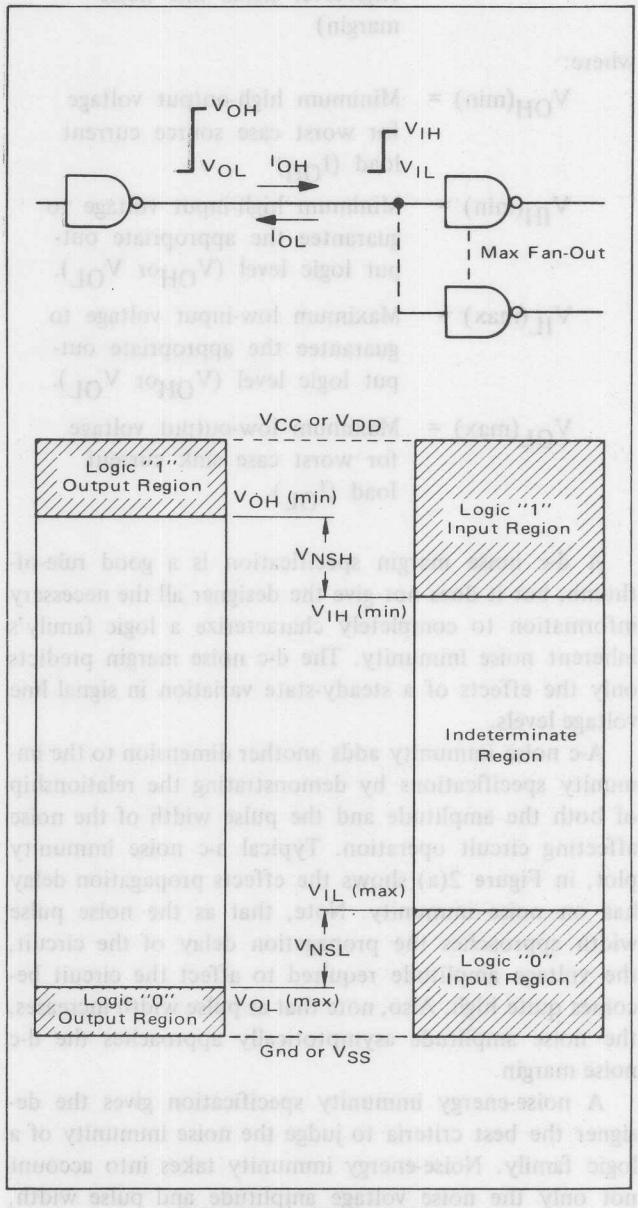


**FIGURE 1 – DC Noise Margin**

## NOISE SPECIFICATIONS

Before comparing the noise immunity characteristics of the different logic families, a discussion of the different types of noise immunity specification is in order. There are three basic ways to specify noise immunity: 1. d-c noise margin 2. a-c noise immunity 3. noise-energy immunity.

The specification, most commonly found on the manufacturer's data sheet, is the d-c noise margin of a circuit. The worst case signal line d-c noise margin of a logic family is shown in Figure 1 and is defined by these equations:

$V_{NSL}(min) = V_{IL}(max) - V_{OL}(max)$ (called low-level signal line noise margin)

$V_{NSH}(min) = V_{OH}(min) - V_{IH}(min)$ (called High-level signal line noise margin)

where:

$V_{OH}(min)$ = Minimum high-output voltage for worst case source current load ($I_{OH}$)

$V_{IH}(min)$ = Minimum high-input voltage to guarantee the appropriate output logic level ($V_{OH}$ or $V_{OL}$).

$V_{IL}(max)$ = Maximum low-input voltage to guarantee the appropriate output logic level ($V_{OH}$ or $V_{OL}$).

$V_{OL}(max)$ = Maximum low-output voltage for worst case sink current load ($I_{OL}$)

A d-c noise margin specification is a good rule-of-thumb, but it does not give the designer all the necessary information to completely characterize a logic family's inherent noise immunity. The d-c noise margin predicts only the effects of a steady-state variation in signal line voltage levels.

A-c noise immunity adds another dimension to the immunity specifications by demonstrating the relationship of both the amplitude and the pulse width of the noise affecting circuit operation. Typical a-c noise immunity plot, in Figure 2(a) shows the effects propagation delay has on noise immunity. Note, that as the noise pulse width approaches the propagation delay of the circuit, the voltage amplitude required to affect the circuit becomes quite high. Also, note that as pulse width increases, the noise amplitude asymptotically approaches the d-c noise margin.

A noise-energy immunity specification gives the designer the best criteria to judge the noise immunity of a logic family. Noise-energy immunity takes into account not only the noise voltage amplitude and pulse width, but also the impedance that coupled noise "sees" on a line. A typical noise energy immunity plot is shown in Figure 2(b) and obeys the formula:

$$E_N = \frac{V_N^2}{R_O} (PW)$$

where:

$V_N$ = noise voltage amplitude required to cause a circuit malfunction

$R_O$ = line impedance (the parallel combination of the circuit output and input impedances on the signal lines, or the return impedance on the power and ground lines)

PW = noise pulse-width

Plot of 2(b) shows the note energy required to effect a circuit reaches minimum value at the point ($PW_{min}E$) where the a-c noise immunity begins bending upward. This minimum value is the point at which noise-energy margin can be most meaningfully specified. The noise-energy curve also could be generated form the a-c noise immunity curve by knowing the characteristic impedance of the line from which the curve was generated.

## THE TEST

Since noise immunity must be approached from a systems standpoint, standard testing for noise immunity must be made under normal logic system operating conditions. Testing of a single gate without considering typical input and output loading factors would not give a true noise figure of merit. Also, testing a large logic system could be impractical. Test circuits that give the best trade-offs between the two extremes, are shown in Figures 3a, b, c, and d and include two gates and a flip-flop from the same logic family. This test gives the designer a good idea how well a logic gate will reject noise under the conditions of typical family input and output loading, propagation delays, and voltage thresholds.

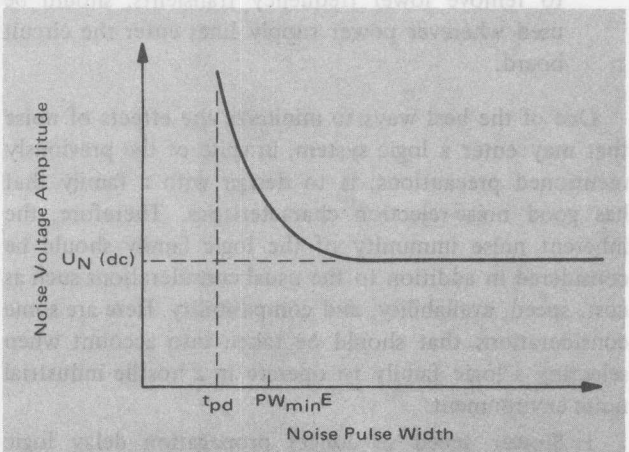


**FIGURE 2a – Typical AC Noise Immunity Plot**

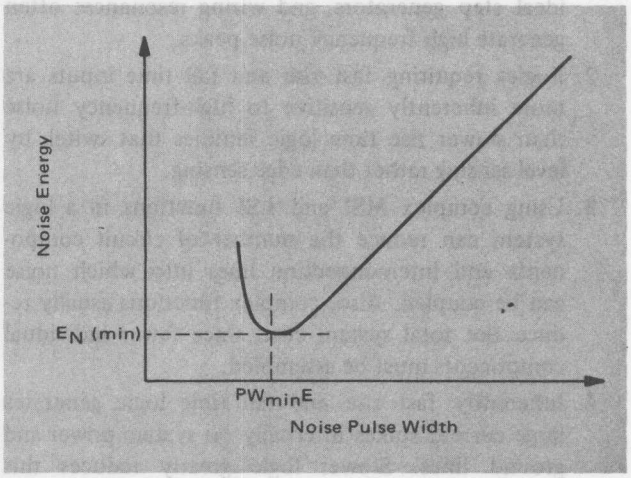


**FIGURE 2b – Typical Noise Energy Plot**

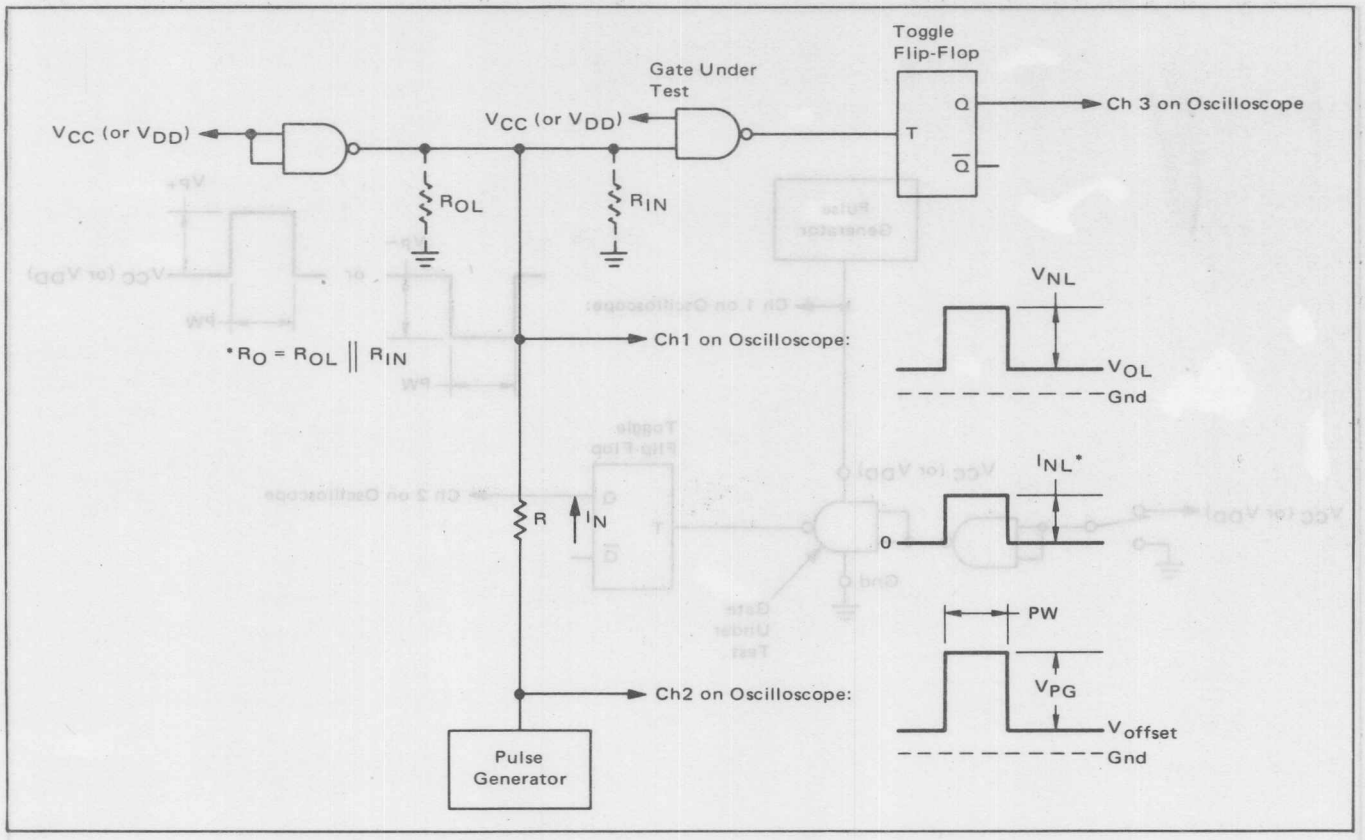


**FIGURE 3a – Low-Level Signal Line Noise Immunity Test Circuit**

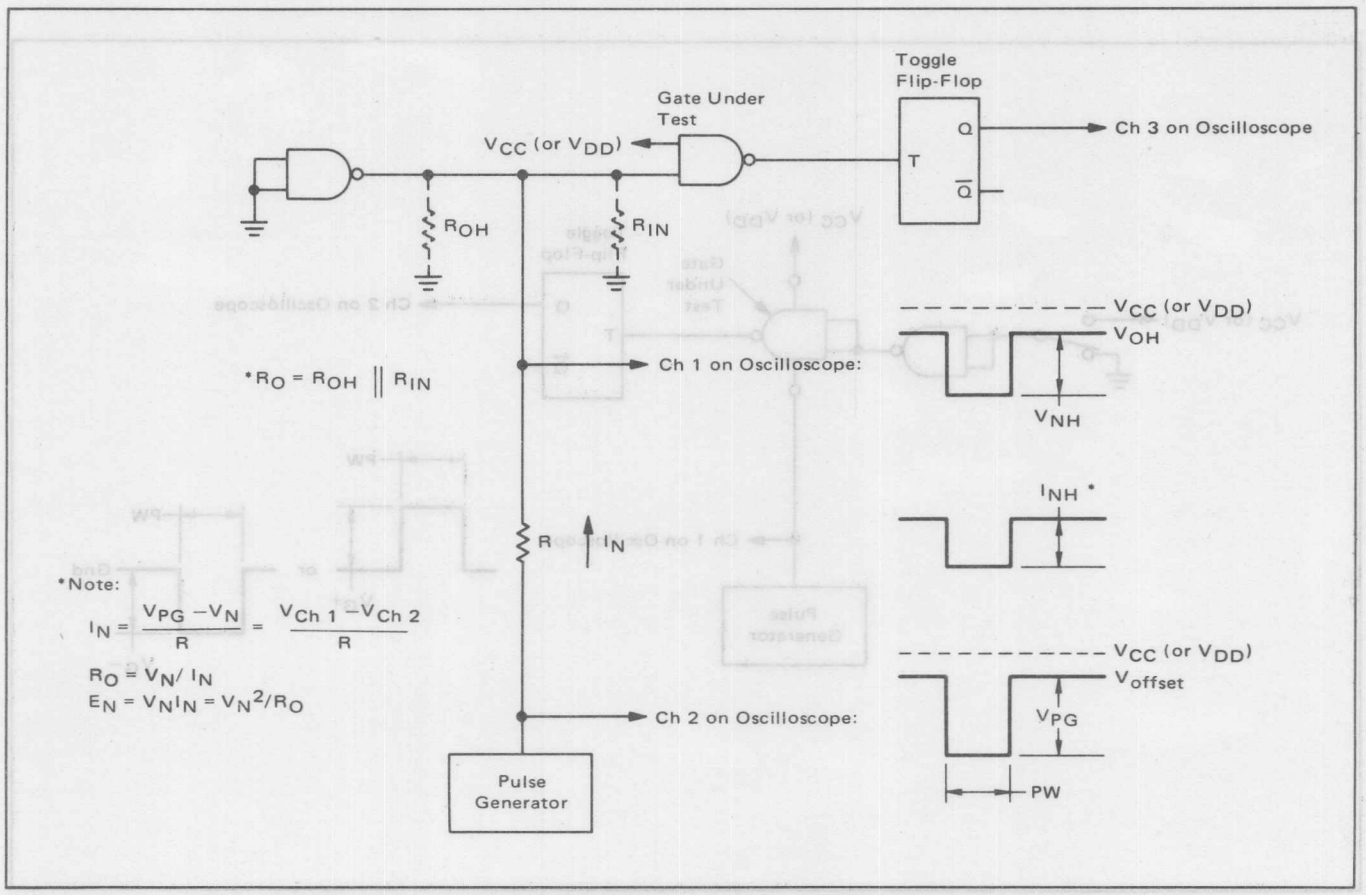


**FIGURE 3b – High-Level Signal Line Noise Immunity Test Circuit**

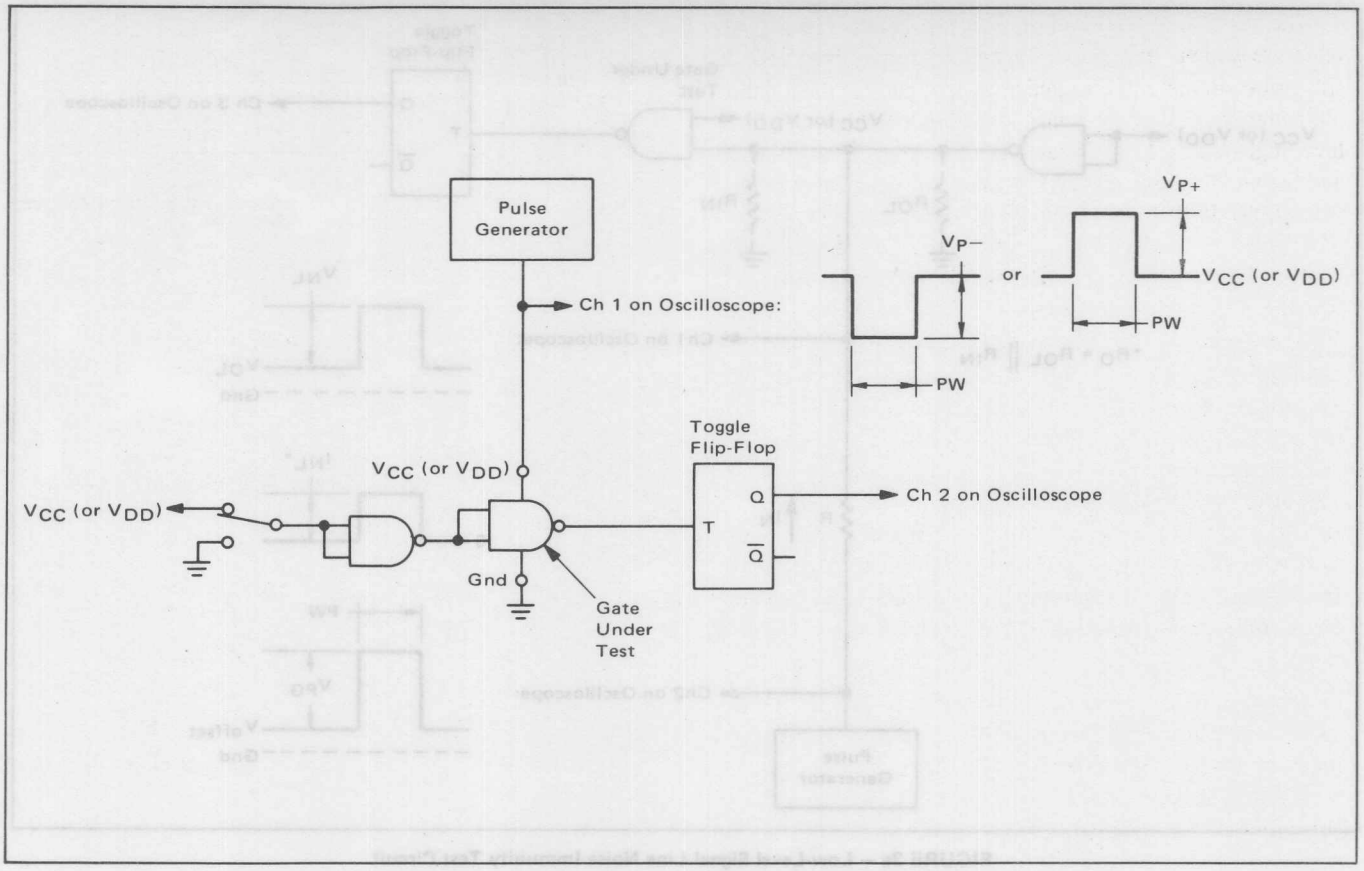


**FIGURE 3c – Power Supply Noise Immunity Test Circuit**

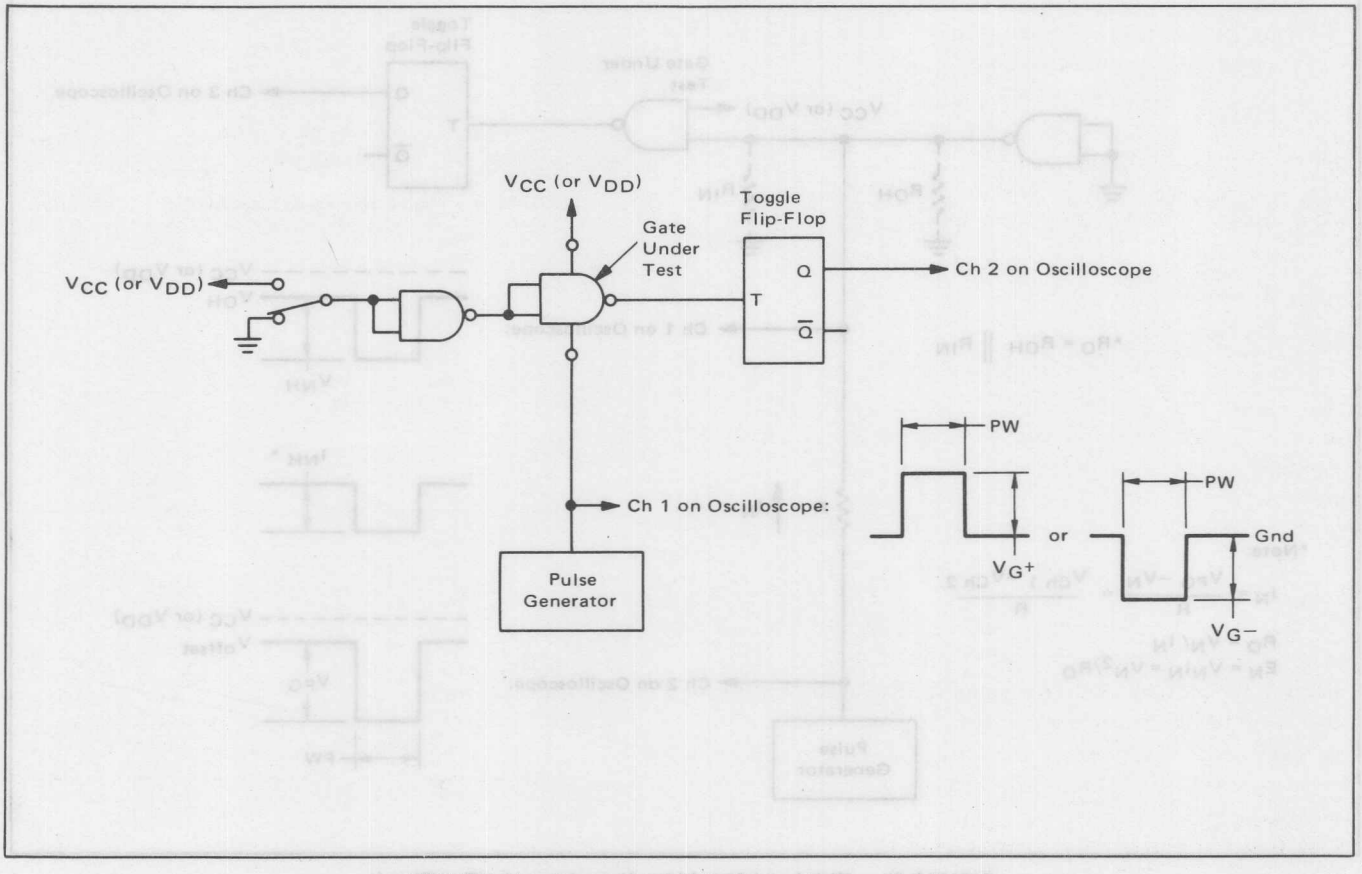


**FIGURE 3d – Ground Line Noise Immunity Test Circuit**

The signal line low-level and high-level noise immunity tests are shown in Figures 3a and 3b respectively. Since the noise margin, line impedance, and propagation delay characteristics of a gate vary between the high and low-level logic states, both states must be tested. Both positive and negative going spikes of noise are generated at the interconnection between the gates using a pulse generator. The pulse generator d-c offset is used to maintain quiescent d-c voltage levels at the interconnection. An oscilloscope is used to measure the pulse voltage amplitude, $V_N$, and current amplitude, $I_N$, necessary to toggle the flip-flop with various noise pulse-widths. From these measurements, the line-impedance and noise-energy margin of a typical gate-to-gate signal-line interconnection can be calculated.

Logic family noise-energy margin concepts that apply to the signal line tests are not directly applicable to the testing of the power and ground lines. This is particularly true in the case of high-impedance MOS logic circuits. Since the impedance, looking into the $V_{DD}$ and $V_{SS}$ terminals, of a CMOS gate is typically $10^9$ - Ohms, the energy required to change the output voltage sufficiently to cause a malfunction is negligible. However, the energy required to raise the voltage level of the low impedance power and ground busses in a practical system can be enormous. Therefore, it is more meaningful to test the noise **voltage level** on the gate power or ground lines that will cause a malfunction. The energy required to produce this voltage is dependent on the power supply output impedance, by-passing precautions taken, and wiring layout and ground return rules employed. The system designer must determine the adequacy of the procedures used. As with the signal line immunity, the supply and ground line immunity is a function of noise pulse width. Depending on the logic state and family type, the logic gate may be sensitive to both positive and negative-going noise pulses on the power and ground lines.

## TEST RESULTS

**Signal-Line Noise Immunity:**

Low-level and high-level signal line a-c noise immunities of the four logic families are shown in Figures 4 and 5. As mentioned previously, the most comprehensive comparisons are taken from plots of relative noise-energy immunity shown in Figures 6 and 7. In these curves the combined effects of voltage threshold, line impedance, and propagation delay on device noise immunity become dramatically clear.

Due to the greater energy scale required, the 15-Volt noise energy characteristics of the CMOS and HTL families are plotted alone in Figure 6. The advantage of low line-impedance becomes clear in this plot. Note that the HTL, with its low-impedance (only 140 Ohms), low-level state, exhibits a minimum noise-energy immunity of 60 nanojoules; this is nearly an order of magnitude greater than the best minimum - that of 15-volt CMOS. Note, however, that the relatively high-impedance (about 1.6K

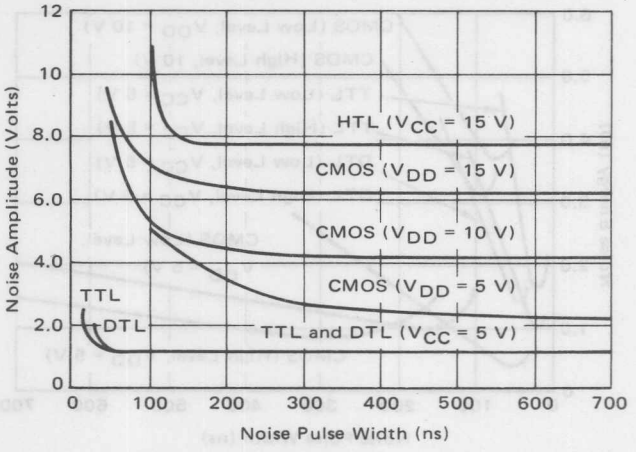


**FIGURE 4 – Low-Level Signal Line AC Noise Immunity**

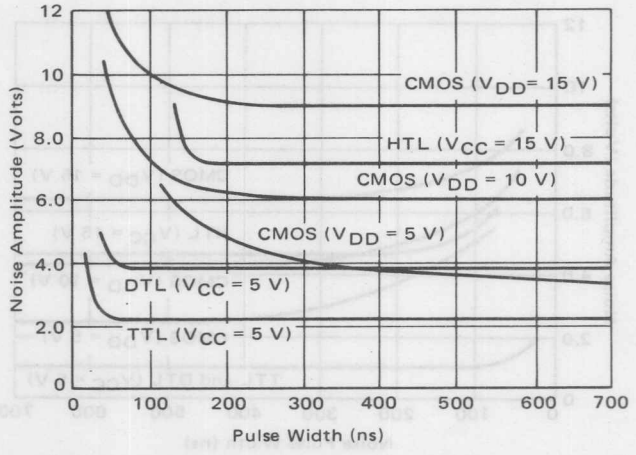


**FIGURE 5 – High-Level Signal Line AC Noise Immunity**

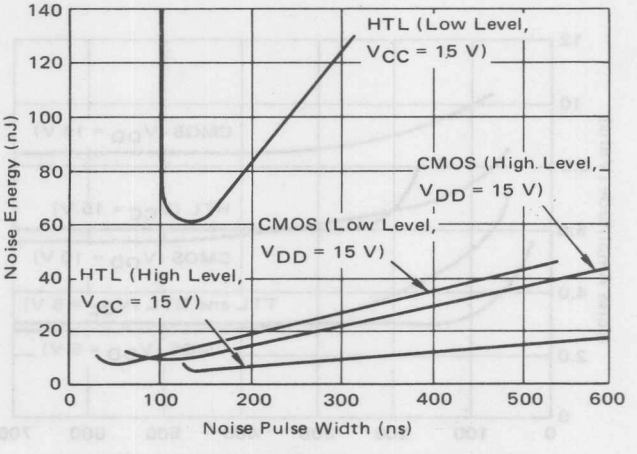


**FIGURE 6 – Signal Line Noise Energy Immunity (CMOS, HTL @ 15 V)**

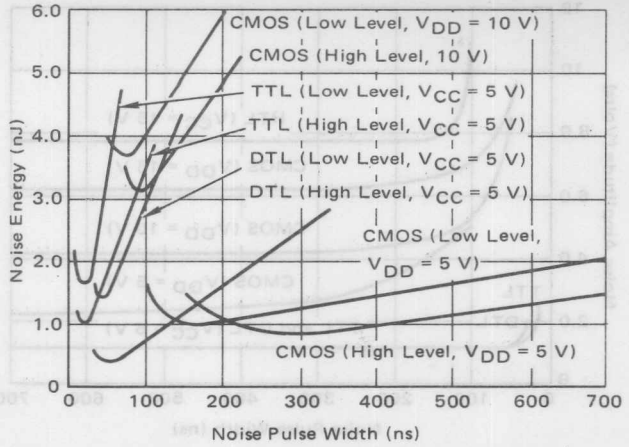


**FIGURE 7 – Signal Line Noise Energy Immunity (CMOS @ 5 V and 10 V; TTL, DTL @ 5 V)**

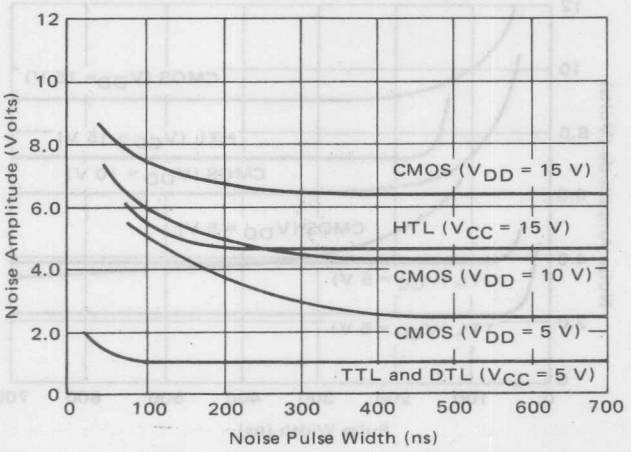


**FIGURE 8 – Ground Line AC Noise Immunity**

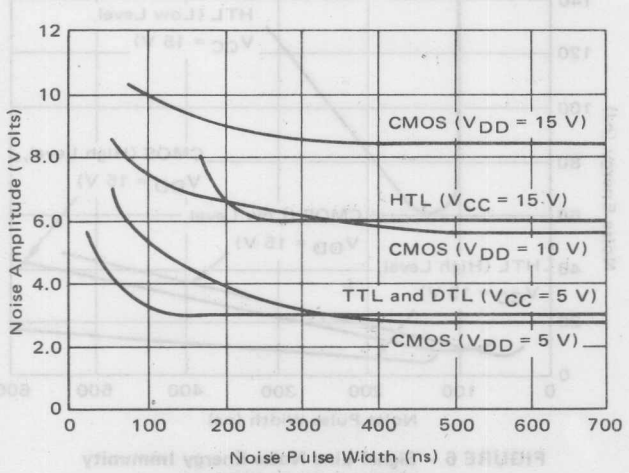


**FIGURE 9 – Power Supply Line AC Noise Immunity**

Ohms) of HTL in the high-level state results in a minimum noise immunity less than that obtained from the 15-Volt CMOS, which has a slightly lower-impedance (about 1K Ohms) and comparable noise-amplitude margins in the high-level state. The HTL does have the additional advantage of slower response time causing the HTL to reach its minimum energy at a wider noise pulse width, and thus to be less susceptible to higher frequency noise then CMOS.

Since the pulse width value indicates the noise frequency to which the device is most sensitive, it becomes clear that not only should the minimum noise energy value be considered, but also the pulse width at which the minimum energy immunity occurs.

This thought must be kept in mind when comparing the noise energy immunity plots in Figure 7 of CMOS at 5 and 10-Volt supply voltages with TTL and DTL at 5 Volts. Low line impedances of TTL devices offer a slight advantage in minimum noise-energy immunity compared to the other devices at 5-Volt power supply levels. TTL high-speed capability does, however, make it much more susceptible to higher noise frequencies than CMOS, which reaches minimum energy immunity value at a much wider pulse width. Even at the higher 10-volt power supply level, CMOS has slower response time than TTL and DTL and at that supply level CMOS also has higher minimum noise energy immunity values. Note that the high-level passive load (about 1.8K ohms) of the DTL family give it the poorest value of noise energy immunity.

**Power and Ground Line Noise Immunity**

The results of the tests for a-c noise immunity on the ground lines of the various logic families are shown in Figure 9: similar results for tests on the power lines are plotted in Figure 10. In general, the graphs show what might be expected: That is, 1.) the CMOS devices operating with a 10 or 15 volt power supply have a much higher typical d-c noise margin and slower response time than the TTL and DTL devices (operating at 5 volts); 2.) CMOS power and ground line noise margin at a 15-Volt supply is higher than HTL (also operating at 15 volts). Even when operating at 10V, CMOS noise margin is comparable to that of the 15-volt HTL devices, although the HTL devices have a noticeably slower response time to noise pulses on the power supply line; and 3.) CMOS d-c noise margin at 5-Volt operation compared to that of the 5-Volt TTL and DTL families, is about the same on the power supply line, and about twice as great on the ground line. However, due to its slow response at that voltage, CMOS exhibits much higher noise immunity than TTL and DTL as noise pulse widths decrease.

It is mentioned in "The Test" section that a device may be sensitive to both positive–and negative–going noise spikes on the power and ground lines. The CMOS devices exhibit a sensitivity to only negative-going noise spikes on the power supply line and to only positive-going spikes on the ground line. The bipolar families, however, showed various degrees of sensitivity to both positive and negative spikes on the power and ground lines depending

| Logic Family | Power Supply (Volts) | Typical Quiescent Power Dissipation (mW) | Typical Propagation Delay (ns) | | Signal Line DC Noise Margin | | | | Typical * Power Supply Line AC Noise Margin (Volts) | Typical * Ground Line AC Noise Margin (Volts) | Typical * Signal Line Impedance (Ohms) | | Typical * Noise Energy Minimum | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | $V_{NL}$ (Volts) | | $V_{NH}$ (Volts) | | | | | | Logic State | | | |
| | | | | | | | | | | | | | Low | | High | |
| | | | $t_{PHL}$ | $t_{PLH}$ | Min | Typ* | Min | Typ* | | | Low | High | $E_{NL}$ nJ | @ PW ns | $E_{NH}$ nJ | @ PW ns |
| DTL (Gate: MC849) | 5.0 | 8.0 | 20 | 50 | 0.7 | 1.2 | 0.7 | 3.8 | 3.0 | 1.0 | 49 | 1.8 K | 1.4 | 45 | 0.4 | 40 |
| TTL (Gate: MC7400) | 5.0 | 10 | 8.0 | 12 | 0.4 | 1.2 | 0.4 | 2.2 | 3.0 | 1.0 | 30 | 140 | 1.7 | 20 | 1.0 | 25 |
| HTL (Gate: MC672) | 15 | 25 | 85 | 130 | 5.0 | 7.5 | 4.0 | 7.0 | 6.0 | 4.5 | 140 | 1.6 K | 60 | 125 | 5.0 | 145 |
| CMOS (Gate: MC14011) | 5.0 | $25 \bullet 10^{-6}$ | 35 | 100 | 1.5 | 2.2 | 1.5 | 3.4 | 2.8 | 1.0 | 1.7 K | 4.8 K | 1.0 | 155 | 0.9 | 280 |
| | 10 | $50 \bullet 10^{-6}$ | 20 | 35 | 3.0 | 4.2 | 3.0 | 6.0 | 5.7 | 4.3 | 670 | 1.5 K | 3.7 | 70 | 3.1 | 90 |
| | 15 | $150 \bullet 10^{-6}$ | 8.0 | 15 | 4.5 | 6.3 | 4.5 | 9.0 | 8.5 | 6.4 | 460 | 1 K | 7.2 | 50 | 8.5 | 75 |

*Typical values are from experimental results of testing a small sample quantity of parts and may not reflect the manufacturer's specifications.

**FIGURE 10 – Tabulated Noise Immunity Results**

on the output logic state of the device under test. Only the worst-case condition is plotted in the graphs of Figures 8 and 9.

Only device power and ground line noise amplitude and pulse width immunities have been discussed. The designer alone has complete control over the impedances on the power and ground lines of his system, and these impedances determine the energy immunity. Significant results of the noise immunity comparisons are tabulated below in Figure 10.

## CONCLUSION

The purpose of this application note was not to sway the reader to use one logic family rather than another based on noise immunity advantages alone. It is meant to be a guide: providing the logic system designer with additional information for selecting a suitable family for a design. No great effort is made to compare the logic families on other important tradeoffs as price, availability, compatibility, MSI functions, power dissipation, operating temperature, power supply range, etc. The task of weighing all of the tradeoffs is necessarily left to the designer, since the relative priority of each of the tradeoffs is based on the system constraints of the design undertaken.

We can conclude however, that logic with good inherent noise immunity can give a system an important advantage when operating in a noisy industrial environment. Hopefully, the information contained here will ease the designer's task in selecting a logic family under noise immunity constraints.

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4. Halligan, J., "Noise Immunity," Engineering Times, March 26, 1973.
5. Boaen, Verell, "Designing Logic Circuits for High Noise Immunity," IEEE Spectrum, p. 53, Jan. 1973.

| Logic Family | Power Supply (Volts) | Typical Quiescent Power Dissipation (mW) | Typical Propagation Delay (ns) | | Signal Line DC Noise Margin | | | | Typical Power Supply Line AC Noise Margin (Volts) | Typical Ground Line AC Noise Margin (Volts) | Typical Signal Line Impedance (Ohms) | | Typical Noise Energy Minimum | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | $V_{NH}$ (Volts) | | $V_{NL}$ (Volts) | | | | | | Logic State | | | |
| | | | $t_{PHL}$ | $t_{PLH}$ | Min | Typ* | Min | Typ* | | | Low | High | Low | | High | |
| | | | | | | | | | | | | | $E_{NL}$ nJ | @ PW ns | $E_{NH}$ nJ | @ PW ns |
| DTL (Data: MC830) | 5.0 | 8.0 | 20 | 50 | 0.7 | 1.2 | 0.7 | 2.6 | 2.0 | 1.0 | 40 | 1.8 K | 1.4 | 45 | 0.4 | 40 |
| TTL (Data: MC7400) | 5.0 | 10 | 8.0 | 12 | 0.4 | 1.2 | 0.6 | 2.2 | 2.0 | 1.0 | 20 | 140 | 1.7 | 20 | 1.0 | 25 |
| HTL (Data: MC872) | 15 | 25 | 85 | 130 | 5.0 | 7.5 | 4.0 | 7.0 | 6.0 | 4.5 | 140 | 1.8 K | 60 | 125 | 5.0 | 165 |
| CMOS (Data: MC14011) | 5.0 | $25 \times 10^{-6}$ | 35 | 100 | 1.5 | 2.2 | 1.5 | 3.4 | 2.5 | 1.0 | 4.7 K | 4.8 K | 1.0 | 165 | 0.6 | 280 |
| | 10 | $80 \times 10^{-6}$ | 20 | 35 | 3.0 | 4.2 | 3.0 | 6.0 | 5.7 | 4.3 | 870 | 1.8 K | 3.7 | 70 | 3.1 | 90 |
| | 15 | $160 \times 10^{-6}$ | 8.0 | 15 | 4.5 | 5.3 | 4.5 | 8.0 | 8.5 | 6.4 | 460 | 1 K | 7.2 | 50 | 8.5 | 75 |

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